Sem VII 'C'-scheme KT Summer 2026 · ECS 04/06/26

Time: 3 hours Max. Marks: 80

N.B. (1) Question No. 1 is compulsory.
(2) Attempt any three questions from remaining five questions.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

Q1. Attempt any four. 20

a. Explain full custom vs semi-custom design flow
b. Write short note on Flash memory.
c. Explain barrel shifter with neat diagram
d. Compare constant field scaling and constant voltage scaling
e. Realize Boolean function F= $\overline{XY + Z}$ by static CMOS and dynamic CMOS logic style.
f. Draw CMOS inverter and explain its operation.

Q2. a) Explain operation of 6T SRAM with read/write circuits. 20
b) Design 4:1 Multiplexer using pass transistor logic and CMOS transmission logic.

Q3. a) Compare static CMOS and pseudo nMOS design styles.
b) Consider a CMOS Inverter circuit with the following parameters. 20
Vdd = 3.3V, Vtn = 0.6V, Vtp = -0.7V, Kn = 200μA/V2, Kp=80 μA/V2
Calculate Noise Margin of the circuit.

Q4. a) Write short note on short channel effects 20
b) Compare high-speed adders (skip, select, save).

Q5. a) Explain working of carry look-ahead adder in detail and its advantages. 20
b) Explain the operation of an SR latch implemented using CMOS logic with a neat circuit diagram.

Q6. a) Draw stick diagram and layout for CMOS based 2 input NOR gate. 20
b) Explain the various components of power dissipation in CMOS circuits. How can power dissipation be minimized?

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