



**ATHARVA COLLEGE OF ENGINEERING
MALAD**

A Report on

64 Bit ALU using FPGA

for

Mini Project 2-B (REV- 2019 'C' Scheme) of Third Year, (TE Sem-VI)

in

Electronics & Telecommunication Engineering

by

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Under the guidance of

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UNIVERSITY OF MUMBAI

AY 2021-2022




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CERTIFICATE

This is to certify that the project entitled **FPGA BASED VIDEO GAME** is a bonafide work of:

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submitted to the University of Mumbai in partial fulfilment of the requirement for the award of **Mini Project 2-B (REV – 2019 ‘C’ Scheme) of Third Year, (TE Sem -VI) in Electronics & Telecommunication Engineering** as laid down by **University of Mumbai** during academic year **2021-22**

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1. INTRODUCTION

1.1 NEED:

An arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic and logic operations. It represents the fundamental building block of the central processing unit (CPU) of a computer. Modern CPUs contain very powerful and complex ALUs. In addition to ALUs, modern CPUs contain a control unit (CU). Most of the operations of a CPU are performed by one or more ALUs, which load data from input registers. A register is a small amount of storage available as part of a CPU. The control unit tells the ALU what operation to perform on that data, and the ALU stores the result in an output register. The control unit moves the data between these registers, the ALU, and memory.

1.2 DEFINITION:

An arithmetic-logic unit is the part of a central processing unit that carries out arithmetic and logic operations on the operands in computer instruction words. We are designing a 64 bit ALU for faster processing speed using FPGA.



2. COMPARATIVE STUDY / LITERATURE SURVEY

ALU is the fundamental unit of a microprocessor which performs all the basic operations based on the control input selection. There are separate units which work independent of the main ALU for performing secondary operations such as address computation. The ALU performs arithmetic functions such as addition, subtraction etc and logic functions including, logic AND, logic OR, and logic XOR etc. These various functions of the ALU are implemented using a set of functional units each implementing a function. It may also be done using sharing of same hardware with use of certain additional units like multiplexers. In this line of thought, the proposed project deals with design and simulation of 64-bit ALU using FPGA with the help of Xilinx ISE software. FPGA is one of the most popular boards in an industry for the modelling, description, and synthesis of digital circuits and systems. It is a high-level board that is difficult to learn, and suitable for the design of complex systems. Also, this board allows users to create complex data types. Design units, also called library units, are the main components of the FPGA. It consists of 4 different notifications which are package, entity, architecture and configuration-component. Also, new library creation and library management which are two of the most valuable features is allowed in Xilinx ISE software.




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3. PROBLEM STATEMENT

Designing a 64-Bit ALU that could perform all possible logical and arithmetic operations with the fastest speed possible.

4. MINI PROJECT DESIGN (PRINCIPLE AND WORKING)

4.1 BLOCK DIAGRAM:

4.1.1 CODE BLOCK DIAGRAM:

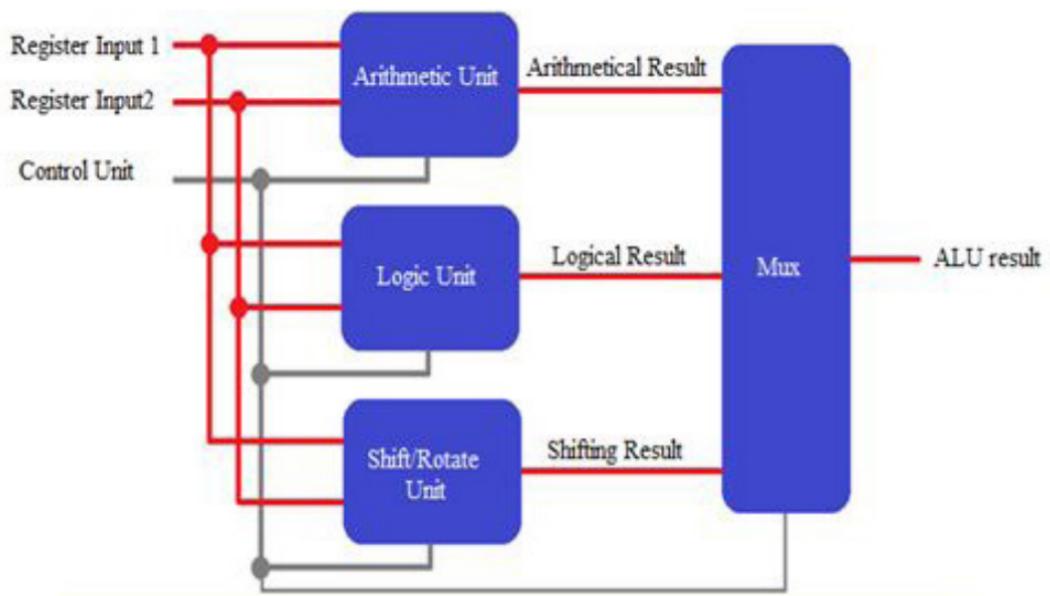


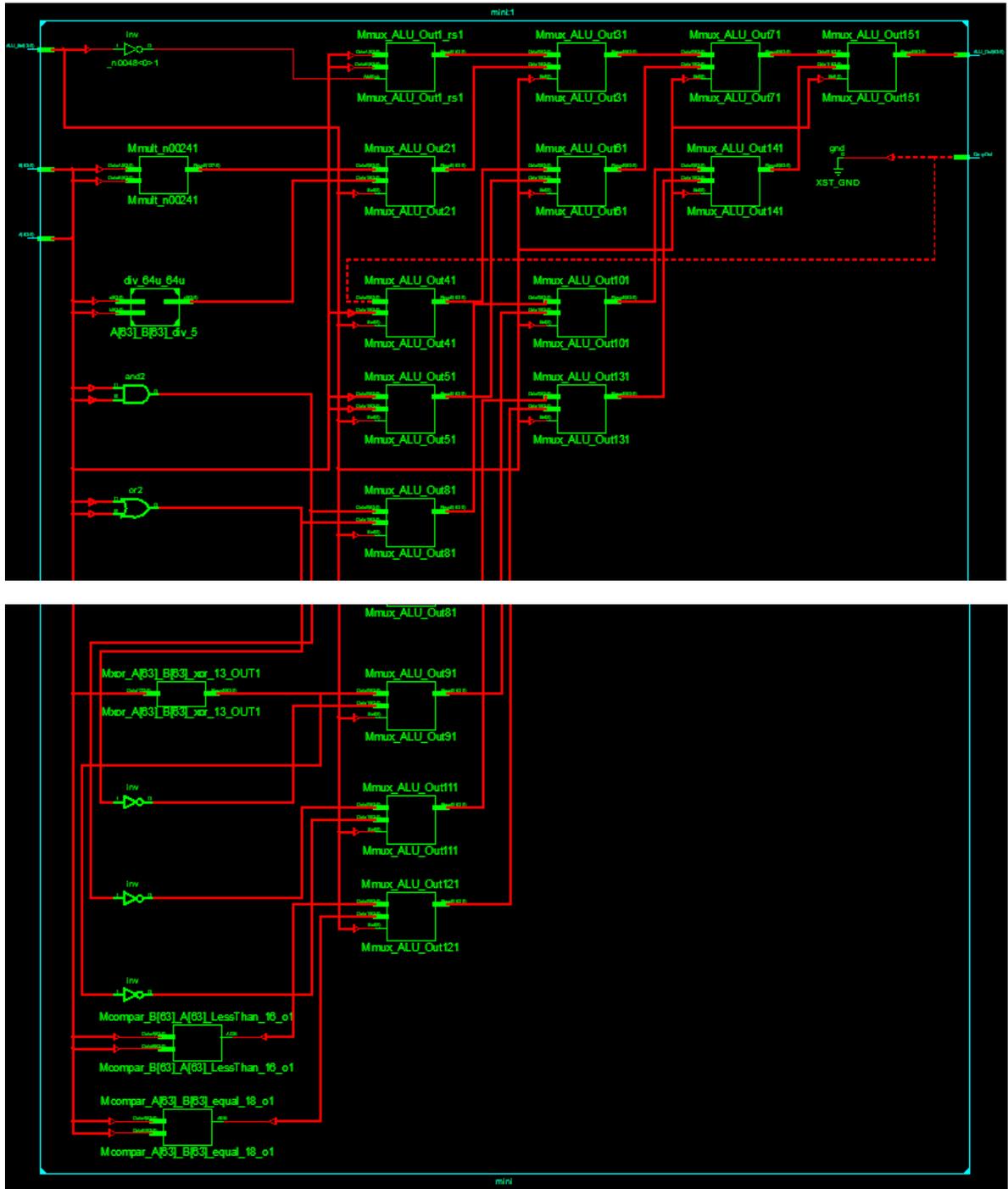
FIG 4.1: CODE BLOCK DIAGRAM

4.2 BLOCK DIAGRAM DESCRIPTION:

4.2.1 CODE:

We declare select line, inputs and outputs first. We assign the each pins for input and output. Then we start with the cases we will have 16 cases because we are using 4 select lines. Each cases have a different operation. After that we give input to the simulated terminal and give input for select line. After we run the code and we get output.

4.3 CIRCUIT DIAGRAM



4.3.1: CIRCUIT DIAGRAM



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4.4 CIRCUIT SIMULATION

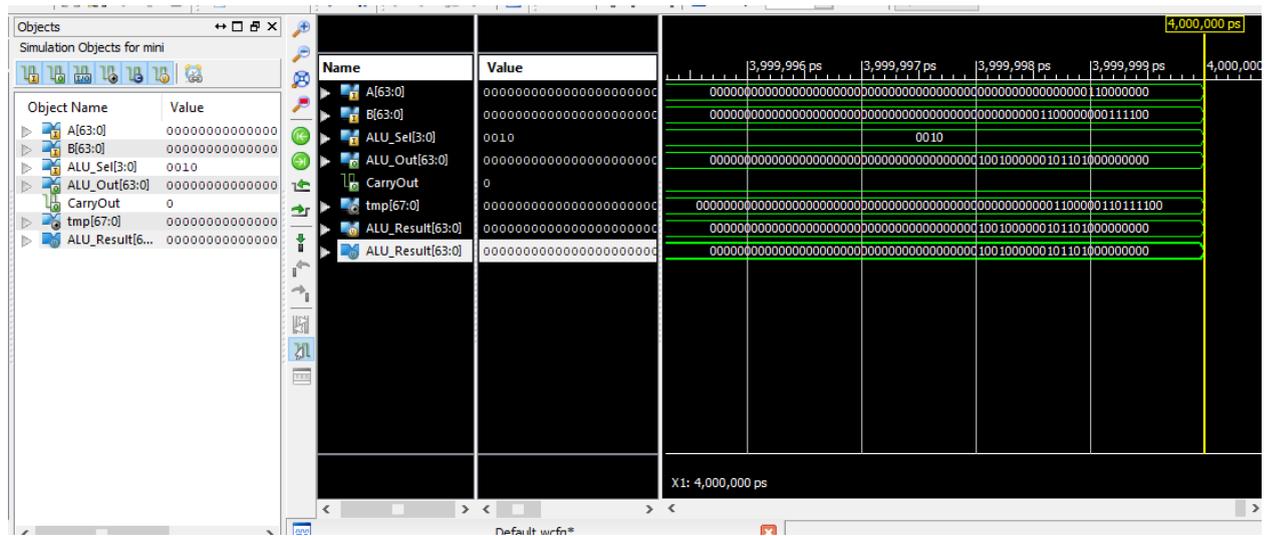


FIG 4.4.1: CIRCUIT DIAGRAM SIMULATION

4.5 WORKING:

Many different studies are given about ALU Design and Implementation with the use of FPGA architecture and VHDL language. In these studies, carry ripple adder (CRA) or carry lookahead adder (CLA) is used in addition operation and unsigned numbers are processed in ALU. Also, Xilinx's software and hardware are used as a development environment as discussed elsewhere. Adder cell is the primary unit of an ALU. Power, speed and area requirements need to be satisfied by the adder cell. The delay in the adder circuit originates from the carry bit calculation. Previous studies used CRA structure in their adder unit. Carry ripple adder is the simplest but the slowest adder structure and constructed by cascading full adders (FA) blocks in series. In the CRA technique, a sequential addition is performed from the less significant bit (LSB) to the most significant bit (MSB) using the FA structures. In this addition, the initial carry bit input is taken as zero during the sum of the LSB bit. While performing the sum of the next two bits, the new carry bit which is calculated from the sum of the previous two bits is used here as a carry bit input. Simulations can be performed manually and directly via Modelism-Altera or indirectly by using the testbench file written in Quartus II. The project is based around the affordable and capable Basys 3 development board which uses a Xilinx Artix-7 series FPGA, with 33k logic cells, and 1800 kbits of block RAM.



Principals
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5. COMPONENTS / TOOLS TO BE USED

5.1 COMPONENTS:

The components that are used for this project are:

5.1.1 SPARTAN 6 DEVELOPMENT BOARD:

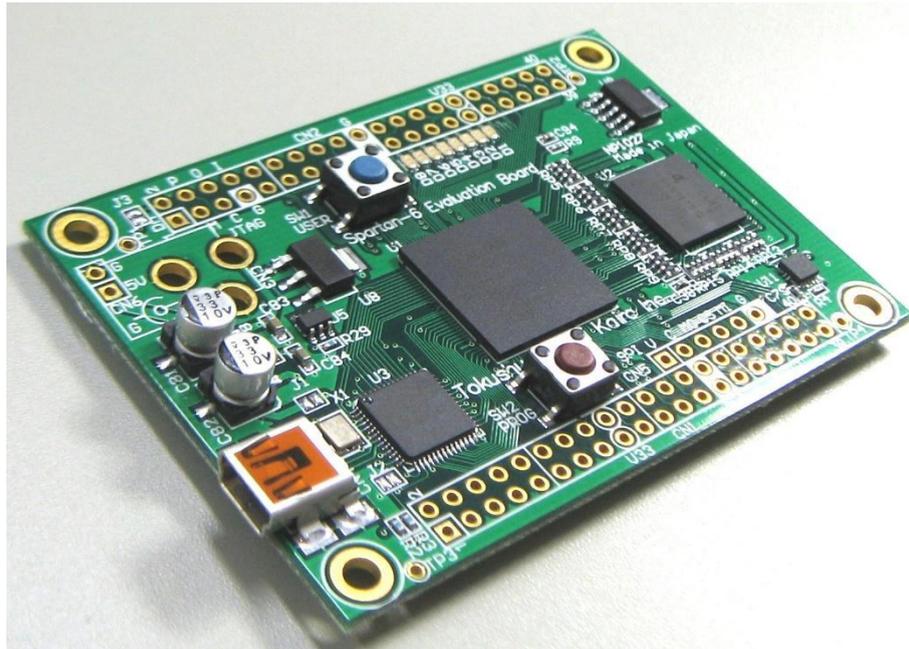


FIG 5.1.1: SPARTAN 6 DEVELOPMENT BOARD

5.2 SOFTWARE:

5.2.1 XILINX:

Xilinx ISE (Integrated Synthesis Environment) is a discontinued software tool from Xilinx for synthesis and analysis of HDL designs, which primarily targets development of embedded firmware for Xilinx FPGA and CPLD integrated circuit (IC) product families. It was succeeded by Xilinx Vivado.




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FIG 5.9: XILINX

6. TROUBLESHOOTING

6.1 PROBLEMS IN PROJECT:

After getting minor error we found out we were using incorrect syntax. This resulted in us not getting any output.

6.2 STEPS TO SOLVE PROBLEMS IN PROJECT:

We found these errors and after a bit of research we changed it to the correct syntax and we got the output.




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7. CONCLUSION

With this project, we can decisively say that an efficient operational unit could be designed with the help of simulation tool and the functional units with optimized count of slices, count of flip-flops and input LUTs. The maximum frequency can be obtained from the analysis of timing view. Power count of the system should be proportional to the respective frequency.




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8. FUTURE SCOPE

In our project, there can be few changes made for the good as we can improve things in the future. The time delay can be optimized using Vedic mathematics technique in implementation of multipliers as the speed of ALU depends prominently on the speed of multiplier. Further in the future work the speed of ALU can be increased by using various fast and efficient multipliers available in the literature.




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