TE Sem V 'C' Scheme . Summer 2025

Duration: 3hrs **[Max Marks: 80]**

EXTC 9/6/25

N.B. : (1) Question No 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

1 Attempt any FOUR [20]

a Define the term Clock skew and its various types.

b For a NMOS transistor if (W/L)=10 $\mu_n C_{ox}$=100μA/V^2 and if Overdrive voltage is 2V then calculate the Value of drain current I_D and Trans conductance gm.

c Draw and Explain the working of NAND based Flash memory.

d Realize 4:1 mux using TG logic.

e Draw the mask layout diagram for PMOS & NMOS transistor using lambda based design rules.

2 a Draw & Explain working of 6T SRAM with its read and write operation. [10]

b Draw and explain the process of fabricating NMOS transistor. [10]

3 a Realize Clocked S-R flip flop using Static CMOS logic and explain the working. [10]

b Draw and explain CMOS inverter with transfer characteristic. Derive the expression for its Threshold voltage. [10]

4 a Draw and explain 4 bit carry select adder along with its advantages and disadvantages. [10]

b Design a 'soda vending machine' using the RTL design process. [10]

5 a Realize the expression $Y = \overline{AB + CD}$ using the following logic style. [10]

1. CMOS logic
2. Pseudo NMOS
3. Dynamic Logic
4. Domino Logic

b Realize the 2 input NAND and NOR gate using CMOS logic. Find equivalent CMOS inverter for simultaneously switching of all input. Assume $(\frac{W}{L})p = 20$, $(\frac{W}{L})n = 15$ [10]

6 a With respect to suitable figure explain the various parasitic capacitors associated with the MOSFET. [10]

b Design 4 *4 bit NOR based memory array and its row decoder to store the following data in respective memory locations. [10]

Memory address	Data
1000	0011
0100	0101
0010	1111
0001	1010

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