



ATHARVA EDUCATIONAL TRUST'S ATHARVA COLLEGE OF ENGINEERING

(Approved by AICTE, Recognized by Government of Maharashtra
& Affiliated to University of Mumbai - Estd. 1999 - 2000)

Department of Electronics & Telecommunication Engineering

Report on

Faculty Orientation Program
for the Department level elective course of
"Mixed Signal VLSI (ECCDLO6011)"

Dated : 14th January 2022

Time: 4:00 – 5:30pm

Organised By: EXTC Department ACE on behalf of Mumbai University

Google Meet Link : meet.google.com/cgw-yqat-mqn

Convener: Mahalaxmi Palinje, I/C HOD-EXTC, ACE

Coordinators: Prof. Joslyn Gracias and Prof. Ruchi Chauhan, EXTC DEPT

Brief Description:

The Board of Studies(BOS) of EXTC of Mumbai university entrusted the organization of Faculty Orientation Program for the Department level elective course of "Mixed Signal VLSI (ECCDLO6011)", the of Third Year, Electronics & Telecommunication Engg., Semester-VI (Rev-2019 C Scheme), A.Y. 2021-22 to the Electronics and Telecommunication Department of Atharva College of Engineering.

The EXTC dept has successfully conducted the online Faculty Orientation Program with the guidance of Prof. Mahalaxmi Palinje, I/C HOD- EXTC and convener. The participants included the EXTC dept faculty from various Engineering colleges affiliated to the Mumbai University..

Resource Person/Speakers:

- 1.Dr.Sudhakar Mande,(BOS Member EXTC),DBIT
- 2.Mr.S.H Mane,VIT
- 3.Prof.Uttara Bhatt, TSEC
- 4.Mrs.Shaista Khanam,VCET

The experienced and skilled resource faculties explained the syllabus of the subject module wise and shared the appropriate textbook to be utilized for the proper coverage of module. Appropriate supporting content like ppts, lab software and experiments were recommended that can be performed by students for better understanding of concepts . All participant doubts and queries were effectively responded.

All participating faculties provides encouraging positive feedback and were presented with e-certificate of attendance.

No. of Participants: 25

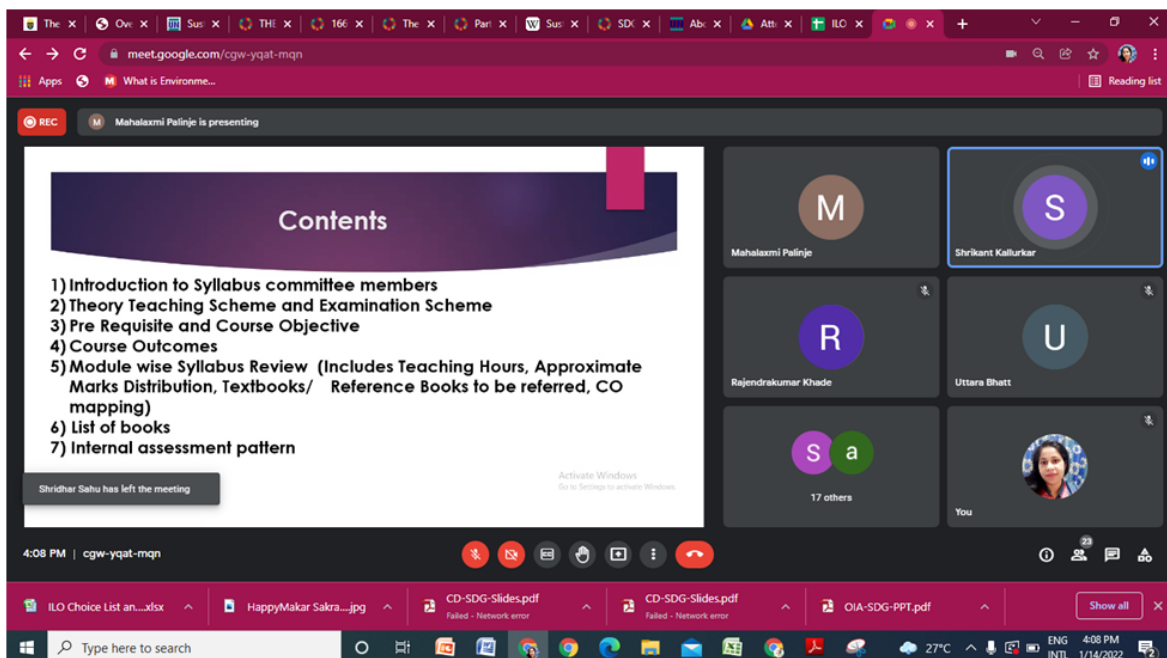
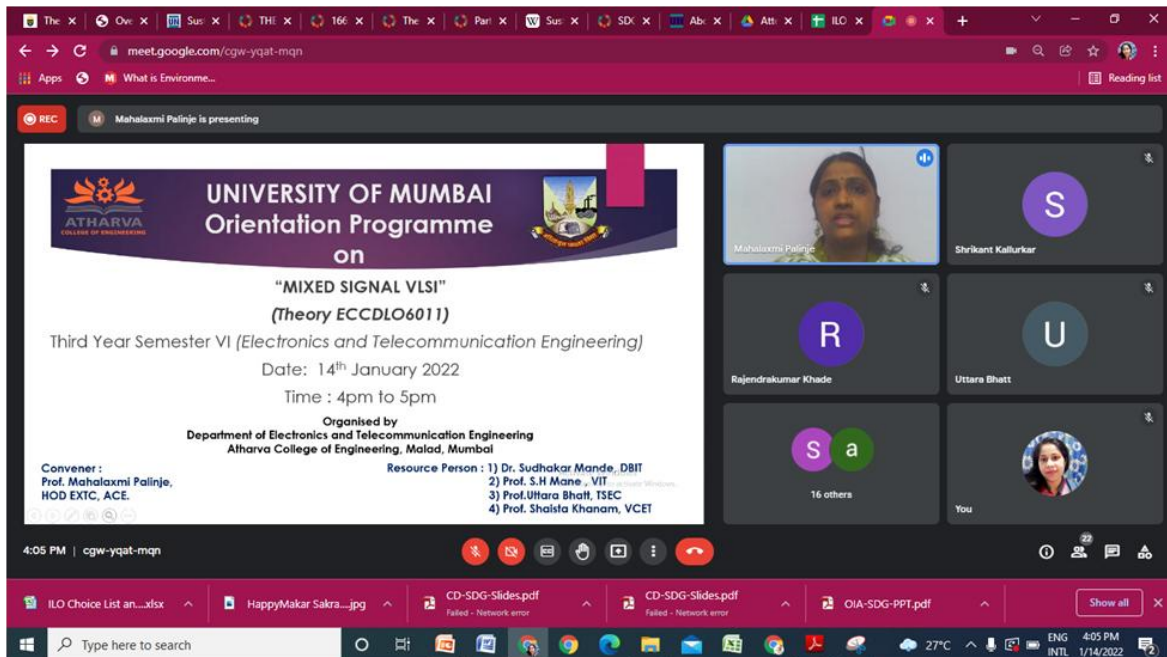


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Photo Gallery



Address :Malad-Marve Road, Charkop Naka, Malad (W), Mumbai 400095, Maharashtra, India



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ECCDLO6011 Mixed Signal VLSI Course Scheme (Theory)

Course Outcomes:

After successful completion of the course student will be able to:

1. Know operation of the various building blocks of analog and mixed signal VLSI circuits.
2. Demonstrate the understanding of various building blocks and their use in design of analog and mixed signal circuits.
3. Derive expression for various performance measures of analog and mixed signal circuits in terms of parameters of various building blocks used to build the circuit.
4. Analyze and relate performance of analog and mixed signal VLSI circuits in terms of design parameters.
5. Evaluate and select appropriate circuit/configuration for given application.
6. Design analog and mixed signal VLSI circuits for given application.

4:21 PM | cgw-yqat-mqn

Module 1. Integrated Circuits Biasing Techniques

- ▶ **1.1 :** Active resistance, current source, current sink, simple current mirror, cascode current mirror [3 Hours]
- ▶ **1.2 :** Current and voltage references, Band gap reference generator [3 Hours]
- ▶ **Shortnote + Derivation + simple numericals**
- ▶ **Recommended – Book Neamen for current mirror**

- ▶ **Duration :** 6 Hrs.
- ▶ **Conceptual and analytical based**
- ▶ **Books :-**
 - 1) Design of Analog CMOS Integrated Circuits, by Behzad Razavi
 - 2) P.E.Allen and D.R.Holberg
- ▶ **Marks in Exam –12 Marks**
- ▶ **CO : 1,2,3**

4:28 PM | cgw-yqat-mqn



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Module 6. Data Converter Architectures

6.1. DAC architectures: R-2R ladder networks, current steering, charge scaling DACs, Cyclic DAC, pipeline DAC, Switched capacitor-based DAC design. **[4 hours]**

6.2. ADC architectures: flash, 2-step flash ADC, pipeline ADC, integrating ADC, and successive approximation ADC, Switched capacitor-based ADC design. **[4 hours]**

Different architecture+ comparison+numericals (5mrks)- sum ,10 mrks- theory

- ▶ Duration : 8Hrs.
- ▶ Conceptual based & Analytical based
- ▶ Books :- Jacob Baker, —CMOS Mixed-Signal circuit designII, IEEE Press, 2009.

Marks in Exam – 16 Marks

▶ CO: 1,2,3

Participants: Uttara Bhatt, Satendra Mane, Mahalaxmi Palinje, Shaista Khan, You.

UNIVERSITY OF MUMBAI
ATHARVA

Orientation Programme on "SIGNAL VLSI" (CCDLO6011)

Third Year Semester VI (Electronics and Telecommunication Engineering)
Date: 14th January 2022
Time : 4pm to 5pm

Organized by
Department of Electronics and Telecommunication Engineering
Atharva College of Engineering, Malad, Mumbai

Convenor : Prof. Mahalaxmi Palinje, HOD EXTC, ACE.

Resource Person : 1) Dr. Sudhakar Mande, DBIT
2) Prof. S.H Mane , VIT
3) Prof Uttara Bhatt, TSEC
4) Prof. Shaista Khan, VCEIT

Participants: Ruchi Chauhan, Mahalaxmi Palinje, Satendra Mane, Sudhakar Mande, You.

Webinar Coordinator

(H.O.D, EXTC)

Principal, ACE.

Prof Joslyn Gracias

Prof Mahalaxmi Palinje

Dr. Shrikant Kallurkar

Prof. Ruchi Chauhan

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