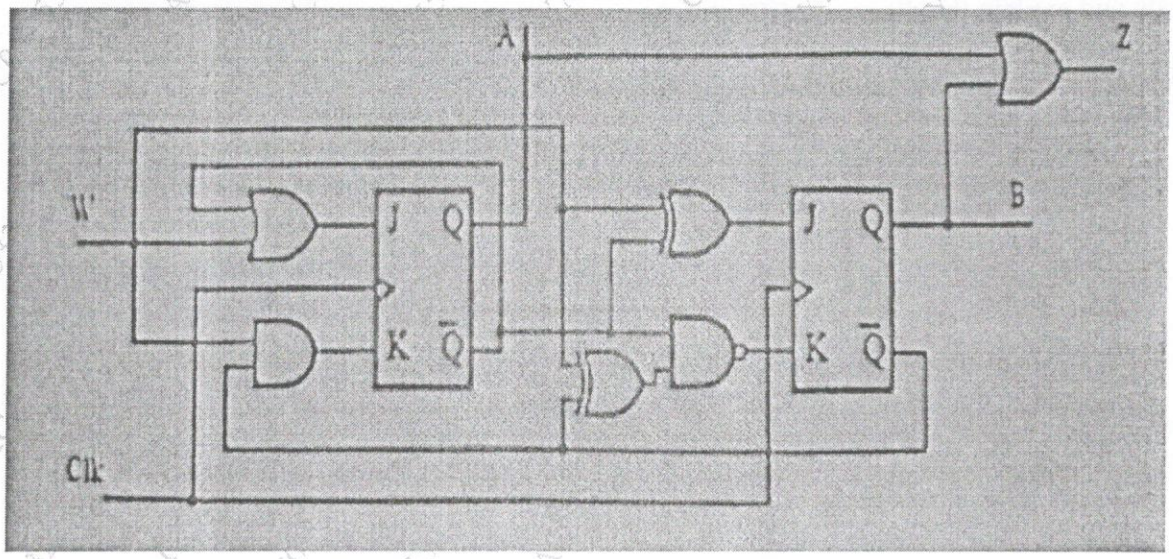
F.E Sem – II (NEP2020) Summer 2025. 20/5/25
(ECS.)

(03 HOURS) (MAX. MARKS : 60)

Note:
1. Question **No. 1** is compulsory.
2. Attempt **any three** questions out of remaining **five** questions.
3. Assume suitable data wherever necessary.
4. Figures to right indicate full marks.

		Marks
Q.1	Answer the following **(Any five)**	
a.	State and Prove DE Morgan's theorem	03
b.	Define the following in terms of Logic families 1. Propagation delay time 2. Noise Margin 3. Power Dissipation	03
c.	Write down truth table of Full Adder.	03
d.	Define Hazards in combinational circuits and List the types.	03
e.	Compare Moore with Mealy circuits	03
f.	Compare CPLD and FPGA	03
g.	What is a shift register? List different types of Shift registers.	03
Q.2 a.	Analyze the circuit given in Figure. Assume initial state as A=0, B=0, Complete table that shows the behavior of this state machine. Is this a state a Moore or Mealy machine? (Explain with a sentence).	10

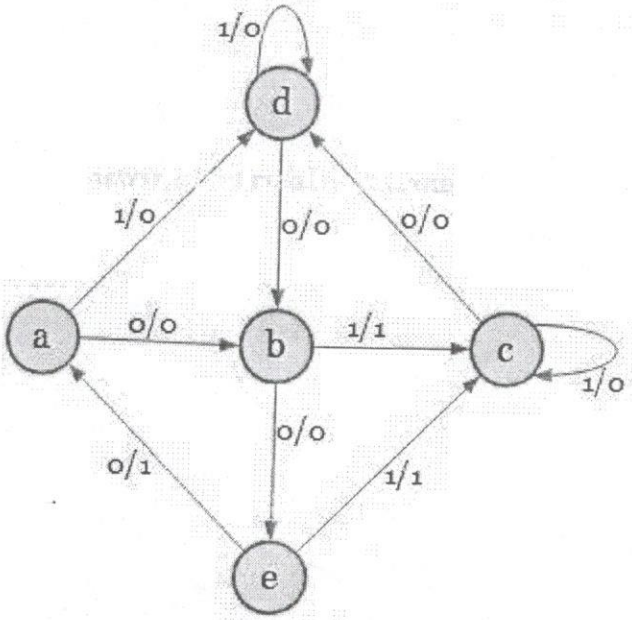


b.	Draw and explain the operation of TTL NAND gate.	05
Q.3 a.	Design a 3-bit synchronous counter using a suitable diagram.	08
b.	Draw K-map for following expression and implement using only Basic gates. $F(A,B,C,D) = \Sigma m(0,2,4,6,8,,10,11,14,15)$	07

Q.4 a. Simplify the following function using Quine –McCluskey minimization technique and implement using gate
$Y(A, B, C, D) = \sum m(0,1\,2, 3, 5, 7, 8, 9, 11, 14)$ **08**

b. What is multiplexer? Give its applications. Design full adder using 4 :1 multiplexer **07**

Q.5 a. Determine the reduced state diagram for the given state diagram. **10**



b. What is ALU? Write its truth table **05**

Q.6 a. Draw and explain the diagram of JK flip-flop using NAND gates. **10**

b. Draw and explain 2-bit magnitude comparator. **05**