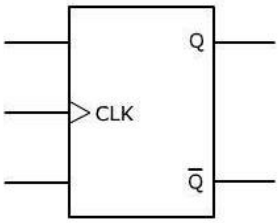
University of Mumbai

Digital Electronics

MCQ

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	When the output will be high for a two input NAND gate?
Option A:	Only if both the inputs are high
Option B:	Only if both the inputs are low
Option C:	Only if one input is high and the other is low
Option D:	If at least one input is low
2.	What is the 2's complement of 5? **(represents-5)**
Option A:	0101
Option B:	1011
Option C:	1010
Option D:	1101
3.	What is the BCD code for $(13)_{10}$?
Option A:	00001101
Option B:	00000111
Option C:	00010011
Option D:	00001011
4.	For Military applications, which TTL series device is used?
Option A:	5400
Option B:	7400
Option C:	4000
Option D:	14000
5.	A three variable expression with variables A, B, C is given as Y=AB+AC+ABC. This expression is in which form?
Option A:	Canonical POS Form
Option B:	POS Form
Option C:	SOP Form
Option D:	Canonical SOP form
6.	How many cells will be present in the K-map of f(A,B,C,D)= πM(2,4,6,7)
Option A:	4
Option B:	8
Option C:	12
Option D:	16
7.	Which logic circuit allows one of the n data inputs at the output?
Option A:	Encoder
Option B:	Multiplexer
Option C:	comparator
Option D:	counter

8.	Which Flip Flop is used to overcome the Race-Around condition?
Option A:	D Flip Flop
Option B:	Master Slave J K Flip Flop
Option C:	S R Flip Flop
Option D:	T Flip Flop
9.	Which type of triggering is represented in the given figure? 
Option A:	Positive edge triggering
Option B:	Negative edge triggering
Option C:	Low level triggering
Option D:	Ultra High level triggering
10.	In which type of registers data are entered or/and taken out in serial form?
Option A:	Asynchronous counter
Option B:	Demultiplexer
Option C:	Shift Register
Option D:	Synchronous Counter
11.	Which of the following is a combinational circuit?
Option A:	Multiplexer
Option B:	Registers
Option C:	Counters
Option D:	Latches
12.	Which Flip Flop is formed if we connect both the inputs of a J-K Flip Flop?
Option A:	D Flip Flop
Option B:	S-R Flip Flop
Option C:	Master Slave J K Flip Flop
Option D:	T Flip Flop
13.	How many resistors are required for an N bit R-2R ladder D/A converter?
Option A:	N
Option B:	2N-1
Option C:	2N
Option D:	N-1
14.	What is the reason to use Dual slope A/D converter in digital voltmeter?
Option A:	Slow speed
Option B:	High accuracy
Option C:	High cost
Option D:	Presence of integrator

15.	What is the minimum time for which the data must be valid before the write pulse ends called?
Option A:	Write pulse time
Option B:	Data hold time
Option C:	Write release time
Option D:	Data set up time
16.	How many chips are required to obtain 1536 X 8 memory using 256 X 8 memory chip?
Option A:	4
Option B:	6
Option C:	8
Option D:	10
17.	In which type of memory access time is different for different locations?
Option A:	Sequentially accessed memory
Option B:	Volatile memory
Option C:	Random access memory
Option D:	Erasable memory
18.	Which is used as the fuse material in programmable ROMs?
Option A:	Silicon
Option B:	Aluminium
Option C:	Nichrome
Option D:	Polycrystalline silicon
19.	Which of the following has a programmable AND array and a Fixed OR array?
Option A:	PAL
Option B:	PLA
Option C:	FPGA
Option D:	CPLD
20.	Which of the following is an advantage of using ROM as a programmable Logic device?
Option A:	Low power requirement
Option B:	Smaller size for large number of inputs
Option C:	Difficult to design
Option D:	Cost is reduced
21.	How many two input AND as well as two input OR gates are required to realize Y= AB + CD + E respectively.
Option A:	2, 2
Option B:	3, 3
Option C:	2, 3
Option D:	3, 2
22.	(315)octal in binary is.....
Option A:	001100010101
Option B:	01101101
Option C:	111101
Option D:	011001101

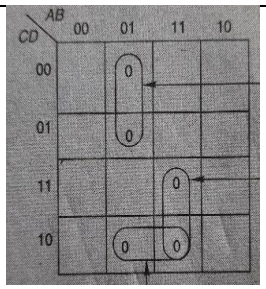
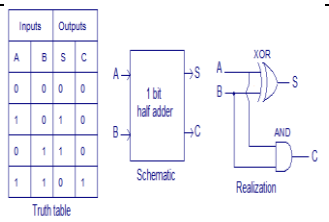
23.	Recommended Fan-Out for standard TTL gate is…..
Option A:	4
Option B:	10
Option C:	50
Option D:	100
24.	Convert BC70.0E hexadecimal to octal
Option A:	136160.035
Option B:	135160.032
Option C:	136160.034
Option D:	136160.34
25.	The Boolean equation, y = (a + b) (a + b+ c+ d) is.....
Option A:	Standard POS equation
Option B:	Standard SOP equation
Option C:	Non-standard SOP equation
Option D:	Non-standard POS equation
26.	How many 16:1 multiplexers are required implement 2 bit binary multiplier
Option A:	2
Option B:	3
Option C:	1
Option D:	4
27.	Full adder adds …….. input bits.
Option A:	2
Option B:	3
Option C:	4
Option D:	5
28.	Gray code of 101010 binary number is…….
Option A:	101010
Option B:	110011
Option C:	111111
Option D:	101011
29.	Out of 8 binary inputs, the circuit will select only one input and pass it on output pin. Which of following circuit will perform this task easily?
Option A:	8:1 Multiplexer
Option B:	3:8 decoder
Option C:	8:3 encoder
Option D:	demultiplexer
30.	The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?
Option A:	0010
Option B:	0000
Option C:	1000

Option D:	1111
31.	MOD 10 counter requires ……flip flops for it's construction.
Option A:	4
Option B:	3
Option C:	2
Option D:	1
32.	Which of following problem may occur in simple JK FF ?
Option A:	Output is invalid, for input values J=K=0
Option B:	Multiple NAND gates required
Option C:	Race around condition
Option D:	Lock Out problem
33.	Resolution of 8 bit DAC in terms of percentage is.....
Option A:	1.587%
Option B:	0.0244%
Option C:	0.392 %
Option D:	6.666 %
34.	A to D converter
Option A:	Converts analog input into digital
Option B:	Converts digital input into analog
Option C:	Converts binary number into decimal number
Option D:	Converts applied input into Gray number
35.	In which of the memory needs periodic refreshing?
Option A:	PROM
Option B:	DRAM
Option C:	SRAM
Option D:	Flash memory
36.	Which of following is Non-volatile memory?
Option A:	Flash memory
Option B:	SRAM
Option C:	DRAM
Option D:	CAM
37.	The storage element for a static RAM is the ……_____.
Option A:	diode
Option B:	resistor
Option C:	capacitor
Option D:	Flip flop
38.	Which of following statement is true about PAL and PLA?
Option A:	Both PAL and PLA contains programmable AND array and programmable OR array
Option B:	PAL has programmable AND array but fixed OR array while PLA has programmable AND array as well as programmable OR array

Option C:	PLA has programmable AND array but fixed OR array while PAL has programmable AND array as well as programmable OR array
Option D:	Both PAL and PLA contains fixed AND array and programmable OR array
39.	FPGA stands for
Option A:	Field Programmable Gate array
Option B:	Free Packet gate Assistant
Option C:	Field Progressive Gate array
Option D:	Field Programmable Grid array
40.	The advantage of using dual slope ADC in digital voltmeter is that
Option A:	Its conversion time is small
Option B:	Its accuracy is high
Option C:	It gives output in BCD format
Option D:	It does not require comparator
41.	Convert (C9.A2)16 hex to octal and decimal
Option A:	(311.100)8 and (201.888)10
Option B:	(311.504)8 and (201.63281)10
Option C:	(311.504)8 and (401.63281)10
Option D:	(671.504)8 and (201.63281)10
42.	As a magnitude comparator, In Binary to gray code converter, IN parity generator, this application of
Option A:	TTL
Option B:	CMOS
Option C:	OR Gate
Option D:	EX-OR Gate
43.	The product term containing all K variables of the function in either complemented or uncomplemented form is called a _____
Option A:	Minterm
Option B:	Maxterm
Option C:	Midterm
Option D:	∑ term
44.	From the below options which one is Disadvantage of CMOS
Option A:	Lower power dissipation
Option B:	High fan out
Option C:	High noise margin for higher values of Vdd
Option D:	propagation delays longer than those of TTL
45.	The expression Y=AB+BC+AC shows the _____ operation.
Option A:	EX-OR
Option B:	SOP
Option C:	POS
Option D:	NOR
46.	There is one difference between a combinational circuit and a flip-flop is that _____
Option A:	The flip-flop requires previous state

Option B:	The flip-flop requires a clock pulse
Option C:	The flip-flop requires next state
Option D:	The flip-flop depends on the past as well as present states
47.	The Master slave flip flop is referred to as?
Option A:	Level triggered flip flop
Option B:	Pulse triggered flip flop
Option C:	Edge triggered flip flop
Option D:	Edge-Level triggered flip flop
48.	How many combinational inputs contain in 3 bits full adder _____
Option A:	3 combinational inputs
Option B:	4 combinational inputs
Option C:	6 combinational inputs
Option D:	8 combinational inputs
49.	A 4-bit ripple counter consists of flip-flops, which each have a propagation delay from clock to Q output of 15 ns. For the counter to recycle from 1111 to 0000, it takes a total of _____
Option A:	60 ns
Option B:	15 ns
Option C:	30 ns
Option D:	45 ns
50.	A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?
Option A:	Tristate
Option B:	End around
Option C:	Universal
Option D:	Conversion
51.	A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains _____
Option A:	0000
Option B:	1111
Option C:	0111
Option D:	1000
52.	A register file holds _____
Option A:	A large number of word of information
Option B:	A small number of word of information
Option C:	A large number of programs
Option D:	A modest number of words of information
53.	What is The full form of PLD is _____
Option A:	Programmable Large Device
Option B:	Programmable Long Device
Option C:	Programmable Logic Device
Option D:	Programmable Lengthy Device

54.	In the design of ----------The programmability and high density of PLDs make them useful.
Option A:	ISAC
Option B:	ASIC
Option C:	SACC
Option D:	CISF
55.	Which memories are if magnetic memory type?
Option A:	Main Memory
Option B:	Secondary Memory
Option C:	Static Memory
Option D:	Volatile Memory
56.	The Volatile memory are refers to _____
Option A:	The memory which loses data when power to the memory circuit is removed
Option B:	The memory whose loosed data is achieved again when power to the memory circuit is removed
Option C:	The memory which loses data when power to the memory circuit is applied
Option D:	The memory whose loosed data is achieved again when power to the memory circuit is applied
57.	How many memory locations are addressed using 18 address bits?
Option A:	165,667
Option B:	245,784
Option C:	262,144
Option D:	212,342
58.	Which signal is sampled at regular intervals for the purpose of ADC?
Option A:	analog signal
Option B:	digital signal
Option C:	quantized signal
Option D:	sampled signal
59.	From the below Which one is not a type of memory?
Option A:	RAM
Option B:	FPROM
Option C:	EEPROM
Option D:	ROM
60.	What is the LSB voltage of an analog to digital converter if the full scale voltage range is 16 volt and the resolution of analog to digital converter in bits is 2?
Option A:	6 volt
Option B:	1 volt
Option C:	4 volt
Option D:	2 volt
61.	The octal number equivalent to hex number(A72E)$_{16}$ is
Option A:	456321
Option B:	123456
Option C:	231456
Option D:	765321

62.	Which is not used in the making of unipolar logic devices
Option A:	CMOS
Option B:	PMOS
Option C:	BJT
Option D:	NMOS
63.	Totem pole in TTL gates is used for
Option A:	To Increase fan out
Option B:	To reduce propagation delay
Option C:	To reduces noise immunity
Option D:	To increase power dissipation
64.	The gate for which the output is true when odd number of inputs are true is
Option A:	OR
Option B:	AND
Option C:	NOR
Option D:	EX-OR
65.	In case of product of sum K-map, each term is called as
Option A:	short term
Option B:	side term
Option C:	Min term
Option D:	Max term
66.	 Identify the logic of the K map given
Option A:	ABC+ACD
Option B:	(A+Bbar+C)(Abar+Bbar+Cbar)(Bbar+Cbar+D)
Option C:	(A+Bbar+C)(Abar+Bbar+Cbar)(Abar+Bbar+Dbar)
Option D:	(A+Bbar+C)(Abar+Bbar+C)(Abar+Bbar+Dbar)
67.	 Given logic circuit can be of
Option A:	Full Adder
Option B:	Half adder
Option C:	Full subtractor
Option D:	Half subtractor

68.	In a 8:1 multiplexer, the number of select input lines will be
Option A:	8
Option B:	4
Option C:	3
Option D:	2
69.	The number of select inputs, m, in a demultiplexer is
Option A:	Same as the number of output lines, n
Option B:	Depends on the number of input lines
Option C:	Related to the number of output lines as $n = 2^m$
Option D:	Related to the number of output lines as $m = 2^n$
70.	The statement not correct for the Quine-Mc-Cluskey method of minimization technique
Option A:	Logic function can be expressed in minterm or maxterm
Option B:	Logic function can be any number of variable
Option C:	Its about finding the prime implicants in each step
Option D:	The method is suitable for computer
71.	Which input is specially used in a demultiplexer tree
Option A:	Select input
Option B:	Clock input
Option C:	Enable input
Option D:	Clear input
72.	A 6 input K map will contain
Option A:	64 cell in one map
Option B:	4 number of 4 variable k map in the 4 cells of 2 variable Kmap
Option C:	6 variable K map is generally not made
Option D:	16 number of 2 variable k map in 16 cells of 4 variable K map
73.	Say which one is not correct: Don t care stage of logic is
Option A:	Useful for the reduction of logic function in maxterm
Option B:	Useful for the reduction of logic function in minterm
Option C:	Used in solution of boolean expression
Option D:	Cannot be used in quine mc-cluskey method
74.	Race around condition arises in
Option A:	S-R flip flop when both the inputs are 1
Option B:	In J-K flip flop when both the inputs are 1
Option C:	In D flip flop when the input is 1
Option D:	T flip flop when the input is 0

75.	State / Inputs Present state | Next state | S | R | J | K | D | T 0 | 0 | 0 | X | 0 | X | 0 | 0 0 | 1 | 1 | 0 | 1 | X | 1 | 1 1 | 0 | 0 | 1 | X | 1 | 0 | 1 1 | 1 | X | 0 | X | 0 | 1 | 0 The table given above is the _____of various flip flop
Option A:	Truth table
Option B:	Characteristic table
Option C:	Excitation table
Option D:	Sequential table
76.	For the faithful reproduction of analog signal, the sampling frequency used in Sample and hold circuit with ADC should be----------if frequency of analog signal is 1000 Hz
Option A:	≥2000 Hz
Option B:	=1800 Hz
Option C:	≤1000 Hz
Option D:	=1000 Hz
77.	For a 4 bits output ADC, the maximum quantization error will be
Option A:	V/4
Option B:	V/8
Option C:	V/16
Option D:	V/32
78.	In a memory in which data can be stored and retrieved in first in first out or last in last out fashion must be
Option A:	Random access memory
Option B:	Flash memory
Option C:	Sequential memory
Option D:	CAM
79.	If the size of address bus and data bus both is 8 bits, the size of memory
Option A:	256 space, each 8 bits
Option B:	8 spaces each 3 bits
Option C:	256 spaces each 3 bits
Option D:	8 spaces each 8 bits
80.	Which is not a PLD
Option A:	Programmable ROM
Option B:	Programmable logic array
Option C:	Programmable array logic
Option D:	Random access memory

1.	Explain the classification of memories based on Physical characteristics and Mode of Access.
2.	Describe the different methods to program Complex Programmable Logic Devices.
3.	Draw dual slope A/D converter with waveforms and list advantages and disadvantages.
4.	What are the drawbacks of R-2R ladder D/A converter? Explain how these drawbacks are overcome in Modified Weighted Resistor D/A Converter and derive the output analog voltage equation for the same.
5.	Explain how a 16 bits ROM array can be used to implement the logic function f(A,B,C,D)=∑m(0,6,9,12,13,15)
6.	Write difference between combinational circuits and sequential circuits.
7.	Write short notes on different logic families (TTL; CMOS).
8.	Differentiate between Multiplexer and Demultiplexer.
9.	Design MOD 6 synchronous counter using T flip flop.
10.	Design two bit comparator. Draw circuit using logic gates.
11.	Draw and explain Memory read cycle
12.	Differentiate between CPLD and FPGA.
13.	Explain the working of successive approximation A/D converter.
14.	Design a 3-bit binary UP/Down counter with a direction control M using J-K Flip Flop.
15.	Design 4 bit Ring counter. Explain with timing diagram.
16.	State and prove De-Morgan's theorem.
17.	State various characteristics of digital ICs
18.	Compare between TTL and CMOS logic.
19.	Convert hexadecimal (A325.2C) to Decimal
20.	Explain master slave JK Flip-flop.
21.	Differentiate between ROM and RAM.
22.	Write note on Parity generator.
23.	Write short note on: Dual slope A to D converter.
24.	Explain different memory write cycle.
25.	Design synchronous 3-bit up counter using JKflip-flop. Design and explain with a suitable diagram, a 4 bit up –down asynchronous counter.
26.	Write a note on PAL. Implement the following using PAL F(A,B,C,D) =∑m(0,1,3,15)
27.	Minimize the four variable logic function using K map in POS form F(A,B,C,D)=∏M(2,4,8,12,14)
28.	Explain with the help of suitable diagram the NAND gate realization using TTL logic
29.	Design synchronous 3-bit up counter using JKflip-flop.
30.	Write a short note on the 3 bits successive approximation A/D converter.
31.	Write a short note on memory mapping and address decoding.
32.	Explain in detail about different ROM programming methods.
33.	Design BCD to 7 segment display with the help of K-map.
34.	Simplify the following using K-map implement using NAND gates

<table>
<tr><td></td><td>$y = \sum m(0,1,2,5,9,13,14,15) + d(4,6,10)$</td></tr>
<tr><td>i.</td><td>Convert
a) $(1011011.11101)_2$ to its equivalent Decimal number
b) $(42351)_{10}$ to its equivalent Octal number</td></tr>
<tr><td>ii.</td><td>Compare NAND, NOR and EX-OR gates in terms of symbol, truth table and logic equation.</td></tr>
<tr><td>iii.</td><td>Realize the given truth table using one 8:1 multiplexer.
<table>
<tr><th colspan="4">Inputs</th><th>Output</th></tr>
<tr><th>A</th><th>B</th><th>C</th><th>D</th><th>Y</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
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