T.E. EXTC SEM V C-scheme KT June 2026. (20)

Duration: 3hrs **[Max Marks: 80]**

08/06/2026.

N.B.: **(1) Question No 1 is Compulsory.**
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

1		**Attempt any FOUR**	**[20]**
	a	State Working of Pass Transistor logic with proper diagram	
	b	Explain Flash memory in brief.	
	c	Explain MOSFET electrical characteristics.	
	d	Write a short note on Interconnect.	
	e	Explain the Barral shifter.	
2	a	Realize a JK flip-flop using CMOS logic and explain its working.	**[10]**
	b	Explain N-MOS fabrication using a neat, clean diagram.	**[10]**
3	a	Consider a CMOS inverter circuit with the following parameters: nMOS V_{TN} = 0.6 V pMOS V_{TP} = -0.7 V Kn = 200 $\mu A/V^2$ Kp = 80 $\mu A/V^2$ Kr = 2.5, V_{DD}= 3.3 V. Calculate noise margin?	**[10]**
	b	Draw and explain a CMOS inverter with a transfer characteristic. Find the condition for a symmetric inverter.	**[10]**
4	a	Draw and explain a 4-bit carry-skip adder along with its advantages and disadvantages.	**[10]**
	b	Design a 'FIR filter design' using the RTL design process.	**[10]**
5	a	Realize the expression $Y=\overline{A+BC}$ using the following logic style. 1. CMOS logic 2. Pseudo NMOS 3. Dynamic Logic 4. Domino Logic	**[10]**
	b	Draw and explain 6-T SRAM with neat and clean diagram.	**[10]**
6	a	Compare the effects of Full scaling and Constant-voltage scaling on Current, Power, and Power density. State which is more power efficient.	**[10]**
	b	Write a short note on : **(Attempt any TWO)** 1. CNFET 2. CLA adder 3. clock distribution	**[10]**

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