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S.E.EXTC SEM III NEP June 2026

(2 hours) (Total Marks: 60)

09/06/2026

N.B.

1. Assume suitable **data** if necessary.
2. Question **No.1 is Compulsory**.
3. Solve any **Three** Questions from **Q.2 to Q.6**.
4. Figures to right indicates **full marks**.

Q.1		Answer any **Five** of the following.	[15]
	A	Construct AND and OR gate using NOR gate.	[03]
	B	Compare CMOS and TTL logic families.	[03]
	C	Perform BCD addition of $(45)_{10}$ and $(37)_{10}$.	[03]
	D	Find the POS form of given function $f = \bar{B}.\bar{C} + \bar{A}.\bar{B} + A.B.C$	[03]
	E	Construct a 8:1 multiplexer using 2:1 multiplexer.	[03]
	F	Compare Mealy and Moore machine.	[03]
Q.2	A	Design Binary to Gray code converter.	[08]
	B	Explain working of decade counter and draw the output waveforms.	[07]
Q.3	A	Implement F (A, B, C, D) = Σ m (1, 4, 5, 7, 10, 12) using 8:1 multiplexer.	[08]
	B	Design a synchronous Mod-12 counter using J-K Flip Flop.	[07]
Q.4	A	What is race around condition in flip-flops? How it is avoided.	[05]
	B	What is shift register? Explain SIPO and PISO with example.	[05]
	C	Write a VHDL code for 4:1 Multiplexer.	[05]
Q.5	A	Explain any practical 3:8 decoder IC.	[05]
	B	Convert D to J-K flip-flop.	[05]
	C	Write a short note on Programmable Logic Array (PLA) and Programmable Array Logic (PAL).	[05]
Q.6	A	Draw and explain BCD adder.	[08]
	B	Draw and explain the working of a 4-bit Ring counter with timing diagram.	[07]

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