15/05/26

FE Sem - II (NEP 2020) ECS Digital Electronics May 2026

[Total Marks: 60]

(Time: 2 Hours)

N.B.: (1) Question No. 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) Each question carries 15 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

1. (a) Compare TTL and CMOS logic families (3)
   (b) Draw symbol, truth table, expression for universal gates. (3)
   (c) Prove that $\overline{((A\bar{B}(C+BD)+\bar{A}\bar{B})C)} = B+\bar{C}$ (3)
   (d) Reduce the following using K-Map technique
   $F = \prod M\,(0, 2, 3, 8, 9, 12, 13, 15)$. (3)
   (e) What is PLD? Explain in detail and Give its advantages. (3)

2. (a) Implement OR using NAND and NOR gate. (08)
   (b) Design and implement a full subtractor circuit. (07)

3. (a) Explain 3-bit asynchronous up-Down counter. (08)
   (b) By using K-Map calculate the minimized expression for the following function and implement it using basic gates. (07)
   $F(A, B, C, D) = \sum m\,(0, 2, 4, 8, 11, 15) + d\,(3, 10, 12, 13)$

4. (a) Implement the function using 8:1 multiplexer $F=\sum m\,(0,2,4,6,8,10,12,14)$ (08)
   (b) Explain in detail S-R and J-K Flip Flops. (07)

5 (a) Differentiate between Mealy and Moore machine (08)
   (b) Explain the working of Bi-Directional Shift Register with a neat diagram and truth table. (07)

6 (a) Define: - (i) Propagation delay time(ii)Noise Margin
   (iii) Power Dissipation, (iv) Fan – in , (v) Fan – out (05)
   (b) Design 2-bit magnitude comparator. (05)
   (c) Design binary to gray code converter using gates. (05)
