S.E. ECS SEM III C-scheme June 2026. (12)

Time: 3 hours

Marks: 80

09/06/2025

N.B.: (1) Question No.1 is compulsory.
(2) Attempt any three questions out of the remaining five.
(3) Each question carries 20 marks and sub questions carries equal marks.
(4) Assume suitable data if required.

Q.1 Attempt Any FOUR **20M**

a. Perform the binary subtraction $(22)_{10}$-$(13)_{10}$ using the 2's complement method. Show all steps clearly (finding 2's complement, addition, and final interpretation of the result).
b. Implement Ex-OR gate using NOR only.
c. Differentiate between wire and reg data types in Verilog with examples
d. Convert a SR Flip-Flop into a D Flip-Flop. Derive the characteristic equation.
e. Explain the difference between TTL and CMOS logic families in terms of technology, power consumption, speed, and noise immunity.

Q.2

a. Realize a 3-to-8 Decoder (IC 74138) using its truth table. Show how it can be used to implement any Boolean function of 3 variables. **10M**
b. Describe the operation modes of IC 74194 Universal Shift Register. Include SISO, SIPO, PISO, and PIPO modes. **10M**

Q.3

a. Implement a Mod-10 (Decade) Counter using JK Flip-Flops. Write the excitation table. Draw the timing diagram for the counter output. **10M**
b. Design a combinational logic circuit to realize the functions: **10M**
F1=AB+C, F2=A+BC
Using PLA. Draw the AND-OR array configuration.

Q.4

a. Design a Mealy machine to detect the sequence 1011 in a serial input stream. Show the state diagram **10M**
b. Write a Verilog module for a 2-to-1 multiplexer using continuous Assignment statements. **10M**

Q.5

a. Design a 3-bit Asynchronous (Ripple) Counter using T Flip-Flops. Draw the timing diagram. Modify it to work as a Down Counter. Show the logic connections. **10M**
b. Write a Verilog module to implement a 4-bit synchronous counter using T flip-flops. **10M**

Q.6 Write short note on

a. Explain the role of Hardware Description Language (HDL) in digital system design. Discuss its advantages, levels of abstraction, and the importance of Verilog. **10M**
b. Explain the working of a Twisted Ring Counter (Johnson Counter) with a neat diagram. Derive the state sequence and discuss its advantages and applications. **10M**

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