



ATHARVA EDUCATIONAL TRUST'S
ATHARVA COLLEGE OF ENGINEERING

(Approved by AICTE, Recognized by Government of Maharashtra
& Affiliated to University of Mumbai - Estd. 1999 - 2000)
Department of Electronics and Telecommunication

REPORT

On

Faculty Orientation Program for “Digital VLSI (ECC503 & ECL 503- Theory and Laboratory”

Date: 10 July 2021

Organised by: Department of EXTC, ACE

Convener: Mahalaxmi Palinje, ACE

Co-Ordinator: Coordinator- Prof. Joslyn Gracias, ACE

Number of attendees: 65 Faculty of different colleges

The Department of EXTC has successfully organized and conducted the ***Faculty Orientation Program* for the course of *"Digital VLSI Theory and Laboratory (ECC 503 and ECL 503)"***, Third Year, Electronics & Telecommunication Engg., Semester-V (Rev-2019 C Scheme), A.Y. 2021-22, on *10th July 2021* on behalf of the University of Mumbai.

Platform: Online, Google Meet

Resource Person/Speakers:

1. Dr. Sudhakar Mande, (BOS Member EXTC), DBIT
2. Mr. S.H. Mane, VIT
3. Mr. Mrugendra Vasmatkar, VESIT
4. Mrs. Shaista Khanam, VCET
5. Mrs. Mahalaxmi Palinje, Convener, ACE

The resource speakers excellently contributed to the session with their detailed explanation and adequate coverage of the syllabus. Appropriate supporting content like books, ppts, lab software and experiments were shared during the session. All participant doubts and queries were effectively responded. The event was attended by over 65 faculty members from various colleges affiliated to Mumbai University.

We would like to thank respected *Hon. Shri. Sunil Rane Sir* (Executive - President of AGI & Founder Secretary - AET) and *Dr. P. N. Nemade sir* (Director-ACE) for their constant support.



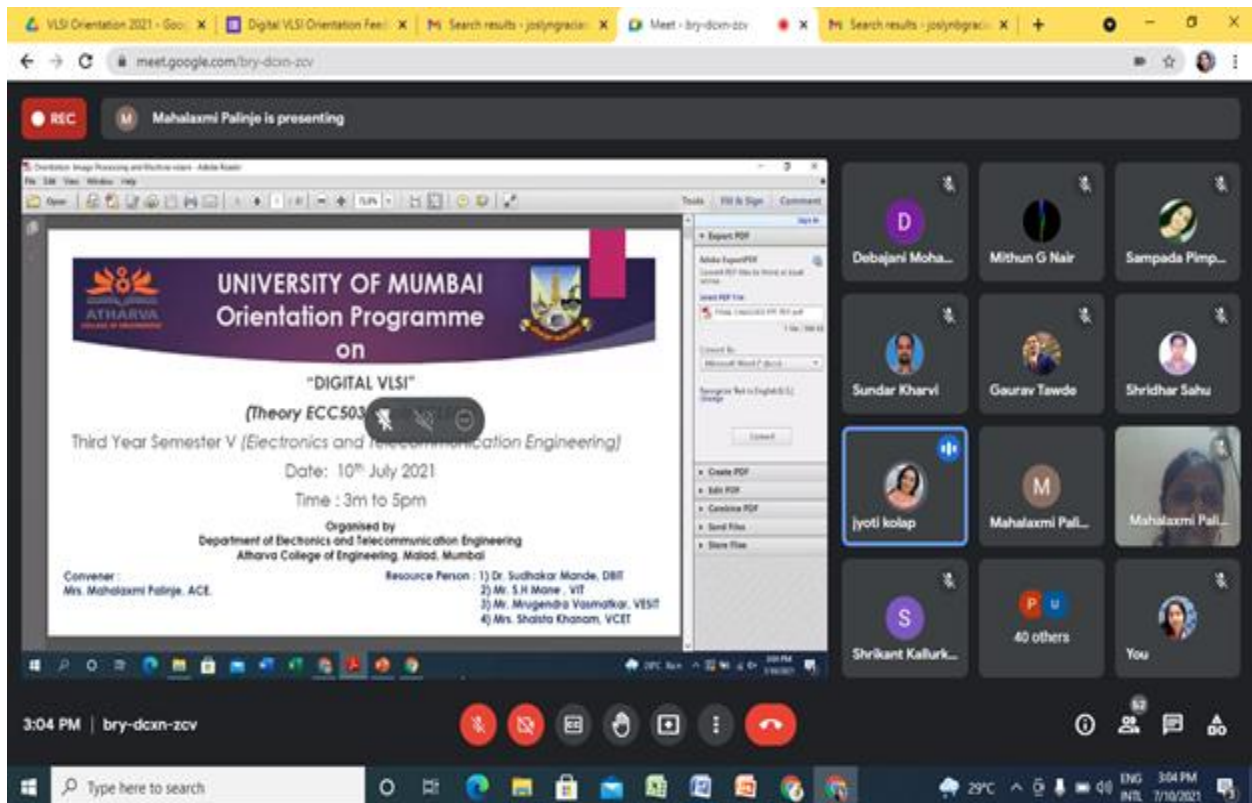
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Also we are grateful to respected *Dr.S.P.Kallurkar sir* (Principal-ACE) and *Prof.Jyoti Kolap mam* (HOD, EXTC) for their guidance and honoring the event with their presence. We extend our appreciation to all faculties of EXTC dept for their motivation and support.

Wishes and Regards,
EXTC Department ACE

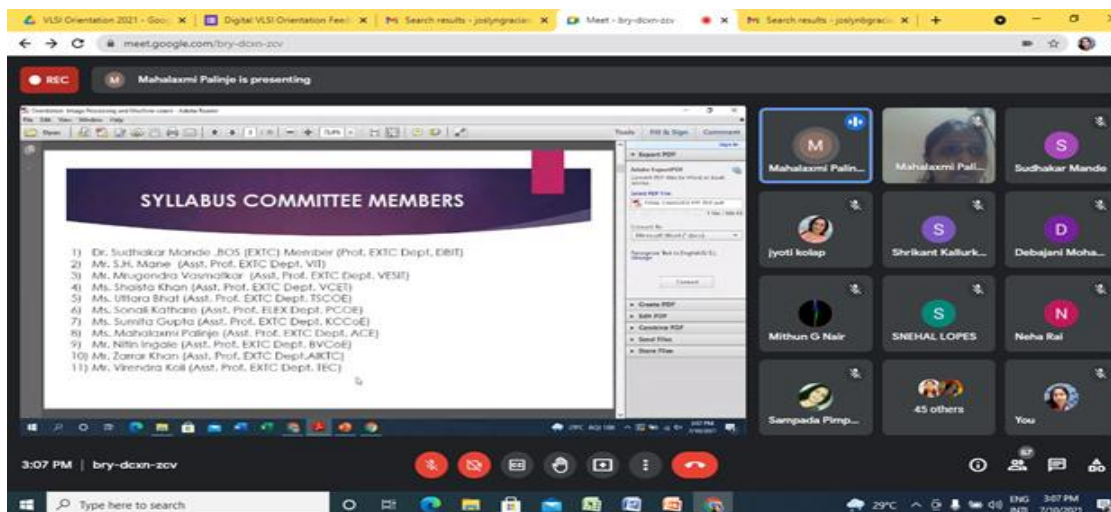
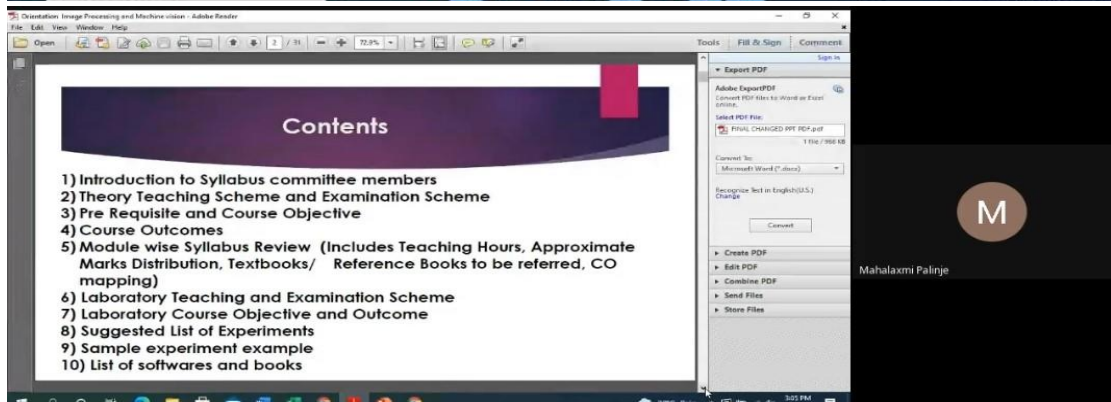
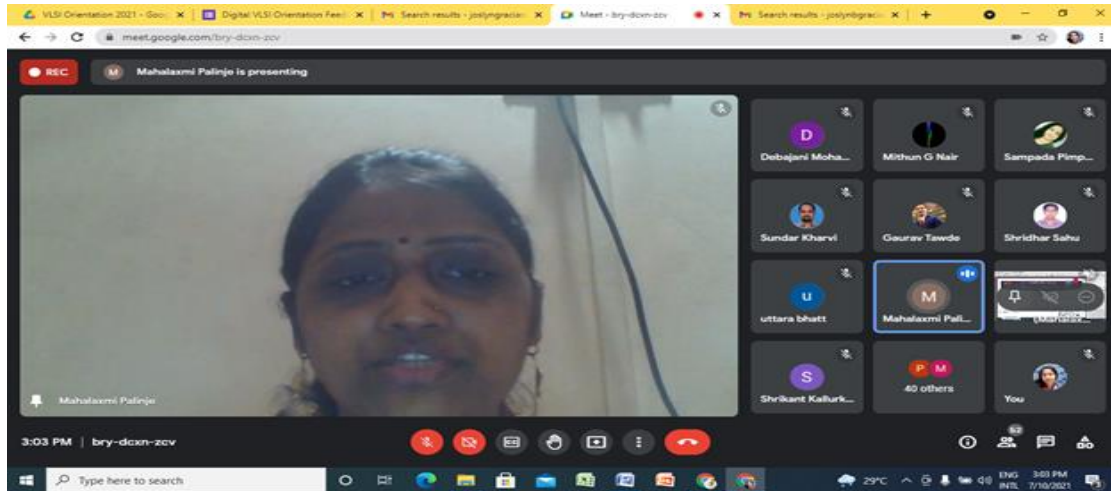
Session Screen shots:





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Module 1. REVIEW OF MOSFET OPERATION & FABRICATION.

- 1.1 : Overview of VLSI design flow, review of MOSFET operation, MOSFET capacitance, MOSFET scaling, SHORT channel effects. [3 hours]
- 1.2 : Fabrication of NMOS & CMOS and LAMBDA based design rules. [3 hours]
- 1.3 : Novel MOSFET : FinFET, GAA-FET, CNTFET. [2 hours]

Duration : 8 Hrs.

- **Conceptual based**
- **Books :-**
- 1) Sung-Mo Kang and Yusuf Leblebici.
- 2) John P. Uyemura.
- 3) Jan M. Rabaey

Marks in Exam – 16-20 Marks

CO : 1.2,3

Module 3. MOS DESIGN LOGIC STYLES

- 3.1 Static CMOS, Pass Transistor Logic, Transmission Gate, Pseudo NMOS, Dynamic Logic, Domino Logic, NORA, Zipper, C2MOS. [4 hours]
- 3.2 Setup time, Hold time, clocked CMOS SR Latch, CMOS JK Latch, MS -JK Flip Flop, Edge triggered D-Flip Flop and realization using design styles [3 hours]
- 3.3 Realization of Shift Register, MUX, design styles ,1-bit

Duration : 9 Hrs.

- **Conceptual and Realization based**
- **Books :-**
- 1) Sung-Mo Kang and Yusuf Leblebici.
- 2) Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic.
- 3) John P. Uyemura.

Marks in Exam –18- 20 Marks

CO : 1.2,5,6

3:42 PM | bry-dcxn-zcv

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The screenshot shows a Google Meet interface with a presentation slide titled "Module 6. RTL DESIGN". The slide content is as follows:

- 6.1. High Level state machines, RTL design process [2hours]**
- 6.2. RTL design of Soda dispenser machine FIR Filter [2hours]**
- Useful links :PPTs**
 - <https://www.cs.ucr.edu/~vahid/dd/>
 - <http://esd.cs.ucr.edu/> (Extra material if you want to review)
- Post for help in teaching RTL design**
 - https://docs.google.com/document/d/e/2PACX:1v15X-eN-c3bNzK2ohDfC9EVrDAAlgd6mpN49U1y1-bFXM09AvITx5_HFN1GWJ16G2NHkM6nz2mT/pub
 - <https://www.youtube.com/watch?v=KDS4hyXoXIs>
 - <http://www.vlsi-expert.com/>
- Duration : 4 Hrs.**
- Design based**
- Books :- Frank Vahid.**
- Marks in Exam – 8-10 Marks**
- CO: 5,6**

The meeting interface shows a grid of participants on the right, including Mahalaxmi Palin, Sudhakar Mande, Jyoti Kolap, Nutan Malakar, Debajani Moha..., Mithun G Nair, SNEHAL LOPES, Neha Rai, and others. The presentation slide is displayed in the main window, and the meeting controls are visible at the bottom.



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The image is a composite of three screenshots. The top screenshot shows a mobile phone interface with a red 'REC' button and a browser window displaying the EDA Playground website. The browser window shows VHDL code for a filter and a VHDL Design section. The middle screenshot shows a desktop window with a SPICE circuit diagram of a CMOS inverter and its corresponding SPICE code. The bottom right corner shows a video call window with a participant named 'Sudhakar Mande'.

NEED TO WRITE SPICE CODE

VTC of CMOS Inverter

```
VDD 1 0 DC 5V
VD 1 4 DC 0V
Mn 3 2 0 0 NMOS W=5U L=1U
Mp 3 2 4 1 PMOS W=10U L=1U
Vin 2 0 DC 5V
.MODEL NMOS NMOS(VTO=1V, KP=100U, LAMBDA=0.01, GAMMA=0.05)
.MODEL PMOS PMOS(VTO=-1V, KP=50U, LAMBDA=0.01, GAMMA=0.05)
.DC Vin 0 5 0.05
.CONTROL
RUN
PLOT V(3)
PLOT DERIV(V(3))
PLOT I(VD)*VDD
.ENDC
.END
```



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The screenshot displays a Google Meet interface. The main window shows a presentation slide titled "ECL503 Digital VLSI Laboratory Course Objectives". The slide content is as follows:

ECL503 Digital VLSI Laboratory Course Objectives

Course objectives:

1. To become familiar with open source circuit simulation tools like Ngspice, Magic etc.
2. To perform various type of analysis of combinational and sequential CMOS circuits
3. To evaluate performance of given combinational and sequential CMOS circuits
4. To design, implement and verify combinational and sequential CMOS circuits using open source VLSI design tools.

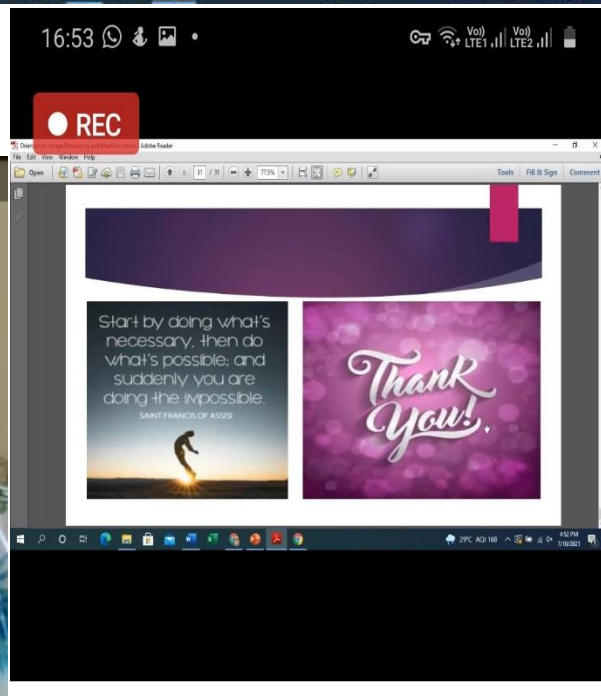
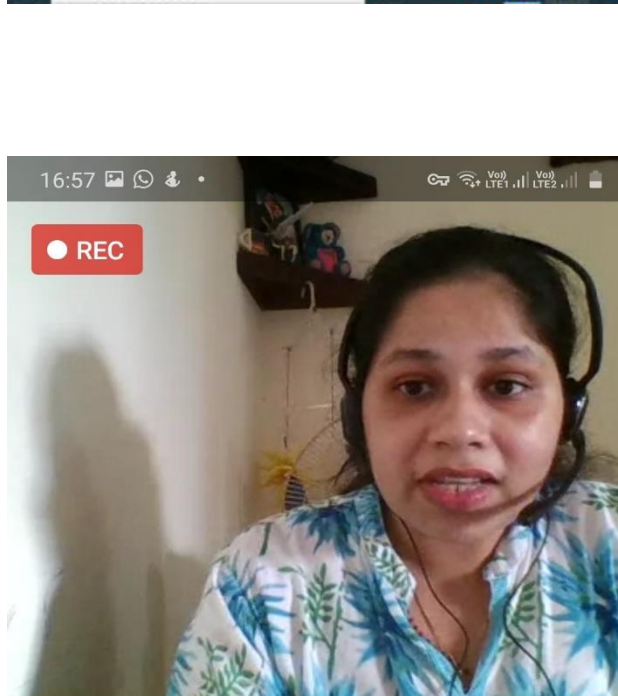
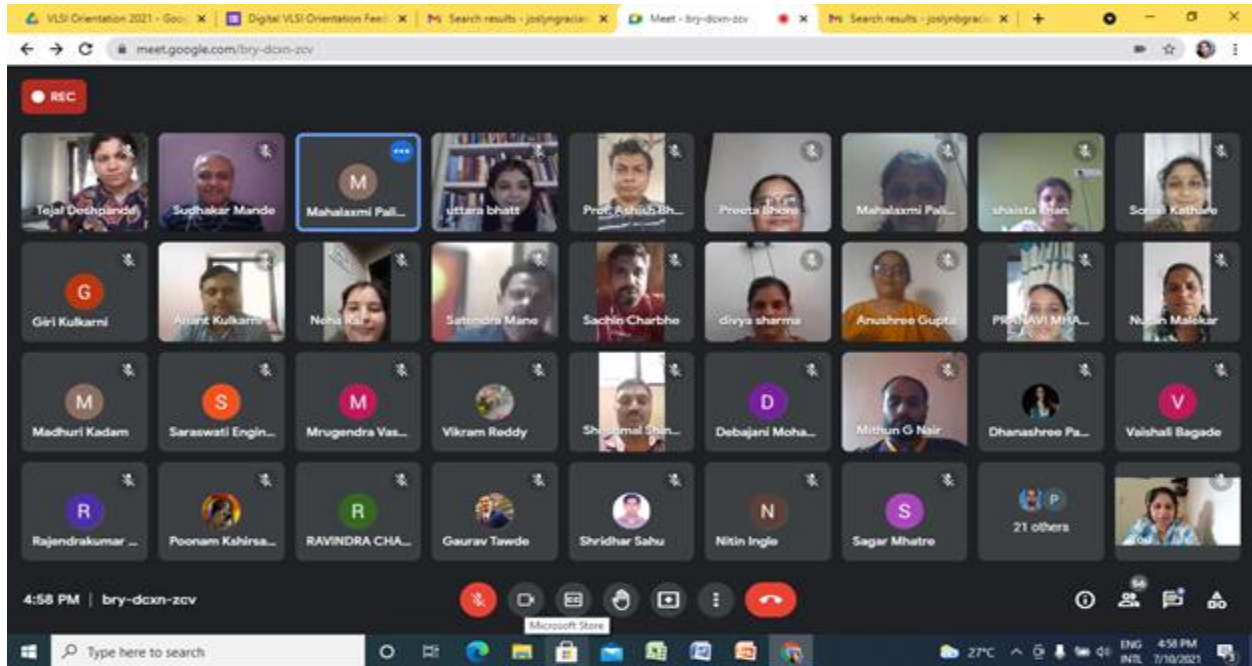
The meeting grid shows 22 participants, including: Tejal Deshpande, Sudhakar Mande, Mahalaxmi Pall..., uttara bhutt, Prof. Ashish Bh..., Preeta Bhofe, Mahalaxmi Pall..., shalika shan, Sonali Kalthure, Giree Kulkarni, Anant Kulkarni, Neha K.S., Sateendra Mane, Sachin Charbho, divya sharma, Anushree Gupta, PINKAVI MHA..., Nuzam Malekar, Madhuri Kadam, Saraswati Engin..., Mrugendra Vas..., Vikram Reddy, Shalika shan..., Debajani Moha..., Mithun G Nair, Dhanashree Pa..., Vaishali Bagade, Rajendrakumar ..., Poonam Kahirsa..., RAVINDRA CHA..., Hemalata Mose, DIPAK JETARA, Mr. Subodh N. P., Sagar Mhatre, and 22 others.

The bottom of the screen shows the Windows taskbar with the time 4:58 PM and date 7/10/2021.



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