Duration: 3hrs **[Max Marks: 80]**

N.B.: (1) Question No 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

1 Attempt **any FOUR** **[20]**

a 1-bit Full adder

b Explain the working of floating gate transistor in Flash memory.

c For enhancement type NMOS transistor threshold voltage V_T=0.6V, μnCox =30 μA/V2, W = 20μm, L = 10 μm. Calculate I_D if for VGS = 1.8 , V_{DS}= 1.8V

d Explain clock generation in VLSI design.

e Draw HLSM of serial FIR filter.

2 a Consider a CMOS inverter with following parameters: **[10]**

nMOS	VTN = 0.6 V	μnCox =60 μA/V2	(W/L)n = 4
pMOS	VTp = -0.7 V	μpCox =25 μA/V2	(W/L)p = 8

Calculate the V_{IL} and V_{TH}. The power supply voltage is VDD = 3.0 V.

b Explain nWell fabrication process with neat diagrams. **[10]**

3 a Realize D flip flop using TG logic and draw its layout. **[10]**

b Explain 3T DRAM with its read and write operation. **[10]**

4 a Realize the expression Y=XNOR using the following logic style. **[10]**

1. CMOS logic
2. Pseudo NMOS
3. Dynamic Logic
4. Domino Logic

b Implement the following **[10]**

1. 4X4 Array multiplier
2. 4-bit carry skip adder

5 a Implement the following **[10]**

1. 4 bit carry lookahead adder carry using CMOS logic.
2. 4- bit barrel shifter.

X532YFE2C5EX532YFE2C5EX532YFE2C5EX532YFE2C5E

b Draw 4 *4 bit NOR based array to store the following data in respective memory locations. **[10]**

Memory address	Data
1000	0101
0100	1101
0010	0010
0001	1011

6 a Design a 'Parallel FIR filter' using the RTL design process. Draw HLSM,FSM, interface and Datapath **[10]**

b Realize the expression Y = A+ BC +F using CMOS logic. Find equivalent CMOS inverter for simultaneously switching of all input. **[10]**

Assume $(\frac{W}{L})p = 15$, $(\frac{W}{L})n = 10$

X532YFE2C5EX532YFE2C5EX532YFE2C5EX532YFE2C5E