Time: 3 Hours **Marks 80**

Note:

1. **Question No 1 is Compulsory.**
2. **Answer any three from the remaining questions.**
3. **Assume suitable data wherever required**

Q1. Solve any four of the following (20)

a. Why MOS Technology has become dominant technology in IC Market.

b. Write a short note on VLSI design Flow.

c. Implement the function F= $\overline{A+(B+C).(D+E)}$ using standard CMOS Logic

d. Implement 4 X 4 NAND based ROM array.

e. Write short on floating gate MOSFET..

Q2.a Compare the full scaling and constant voltage scaling models of MOSFET. Demonstrate the effects of scaling on the area, delay, power consumption and current density of the device. (10)

b. Explain CMOS inverter characteristics mentioning all regions of operation. (10)

Q3.a Compare Pass transistor logic, NMOS logic and CMOS logic. (10)

b. Draw1T DRAM cell and explain its read write and refresh operation (10)

Q4.a Compare Static CMOS and Pseudo NMOS design styles. Implement 2 input NOR gate using pseudo NMOS design style. (10)

b. Draw and explain the 4 *4 Barrel Shifter (10)

Q5.a Draw D flip flop using CMOS logic and explain the working. (10)

b. Explain 4:1 Multiplexer using NMOS pass transistor. Explain the advantages of using Transmission gates. (10)

Q6. Explain any four (20)

a. BJT and MOS Technologies

b. LATCH UP in CMOS

c. Sense Amplifier.

d. Power dissipation in CMOS

e. ZIPPER logic design style
