

Duration: 3hrs

[Max Marks:80]

- N.B. : (1) Question No 1 is Compulsory.
 (2) Attempt any three questions out of the remaining five.
 (3) All questions carry equal marks.
 (4) Assume suitable data, if required and state it clearly.

- 1 Attempt any FOUR [20]
 a Explain significance of clock gemneration in VLSI design.
 b For enhancement type NMOS transistor threshold voltage $V_T=0.6V$, $V_{GS} = 3.3V$, $V_{DS}= 2$, find transistor is operating in saturation or Linear region.
 c Draw and Explain the working of NAND based Flash memory.
 d Realize 2:1 mux using TG.
 e Draw layout of Inverter using lambda based design rules.
- 2 a Explain 1T DRAM with its read and write operation, also draw the layout. [10]
 b Explain nMOS fabrication process with neat and clean diagrams [10]
- 3 a Realize the following [10]
 1) SR latch using CMOS 2) DFF using TG
 b Draw and explain CMOS inverter with transfer characteristic. Find the condition for symmetric inverter. [10]
- 4 a Implement 1) 8-bit carry select adder 2) 4-bit array multiplier [10]
 b Using the RTL design process [10]
 1) Design Datapath of Parallel FIR filter
 2) Design HLSM for Soda dispenser machine
 3)
- 5 a Realize the expression 1-bit full adder using the following logic style. [10]
 1. Pseudo NMOS
 2. Dynamic Logic
- b Realize the 2 input NAND and NOR gate using CMOS logic. Find equivalent CMOS inverter for simultaneously switching of all input. Assume $(\frac{W}{L})p = 20$, $(\frac{W}{L})n = 15$ [10]
- 6 a Compare the effect of Full scaling and Constant voltage scaling on Current, Power, power density. State which is more power efficient [10]
 Draw 4 *4 bit OR based array and NOR based array to store the following data [10]
 b in respective memory locations.

Memory address	Data
1000	1100
0100	1001
0010	0110
0001	1011
