Time: 3 hours **Max. Marks: 80**

N.B. 1) Question No. 1 is compulsory.
2) Attempt any three from the remaining questions.

1 Solve the following questions:

a) State and prove Demorgan's theorem with the help of proper example. **5**

b) Represent the decimal number 27 in binary form using **5**
1) Binary code 2) Gray code **5**

c) Explain working of universal shift register with the help of different operating modes. **5**

d) Design 4:1 multiplexer using VHDL/Verilog code.

2 a) i) Convert the following binary numbers to their decimal equivalent numbers. **10**
1) 10010111 2) 10111.0110
ii) Convert the following decimal numbers to their binary equivalent numbers.
1) $(79.515)_{10}$ 2) $(109.125)_{10}$

b) Simplify the following three-variable expression using Boolean algebra. **10**

i) $Y(A, B, C) = \sum m(0, 1, 3, 4, 7)$

ii) $Z(A, B, C) = \sum m(0, 1, 2, 3, 4, 5, 6, 7)$

3 a) Simplify the following four-variable Boolean functions using Quine-McCluskey method. **10**
$Y(A, B, C, D) = \sum m(2, 4, 5, 9, 12, 13)$

b) i) Convert S-R Flip-Flop to T Flip-Flop. **10**
ii) Convert J-K Flip-Flop to T Flip-Flop.

4 a) Simplify the following Boolean expressions using K-map and implement obtained expressions using suitable gates. **10**
i) $Q(A, B, C, D) = \pi M(1, 2, 5, 6, 8, 9, 15)$
ii) $R(A, B, C, D) = \pi M(0, 1, 2, 3, 5, 6, 7, 12)$

b) Differentiate between PAL (Programmable Logic Array) and PLA (Programmable Array Logic) with the help of suitable example. **10**

5 a) Design and explain 2-bit magnitude comparator. **10**

b) Prove that NAND and NOR gates are universal gates **10**

6 a) Explain working of PISO (Parallel Input Serial Output) and SIPO (Serial Input Parallel Output) types of shift registers. **10**

b) Implement half subtractor using suitable gates **5**

c) Design 8:1 Mux using 4:1 Mux. **5**

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