

Duration: 3hrs

[Max Marks:80]

Note:

- 1) Question No 1 is Compulsory.
- 2) Answer any three from the remaining questions.
- 3) Assume suitable data wherever required

- Q1. Solve any four of the following (20)
- a. Compare Constant Voltage Scaling and Full Scaling with respect to Threshold Voltage, Doping densities, Oxide capacitance, Drain current and Power density
 - b. Explain the impact of variation of Load resistor on Voltage Transfer Characteristics (VTC) of the Resistive Load Inverter.
 - c. Implement NAND based SR Latch circuit using CMOS and also using depletion load nMOS.
 - d. What is switching power dissipation? What are the different means for reducing the same?
 - e. Compare Full custom and Semicustom IC Design flow
- Q2.a Draw and explain the Voltage Transfer Characteristics of CMOS inverter. Write the noise margin formulae. Also draw VTC showing the impact of variation of K_R (i.e. K_n/K_p) for $K_R < 1$, $K_R = 1$ and $K_R > 1$. (10)
- b. With the help of suitable diagram, explain the cascading problem in dynamic CMOS logic? Explain how this limitation is overcome. (10)
- Q3.a What are the advantages of using transmission gates over pass transistors? Implement 4:1 MUX using pass transistor logic (10)
- b. Compare Static CMOS and Pseudo NMOS design styles. Implement the logic function $F = (A + B + C) \cdot (D + E)$ using static CMOS design style as well as Pseudo NMOS design style. (10)
- Q4.a Explain the significance of High-speed adder in Data Path design. Explain any one scheme for high-speed adders. (10)
- b. State the difference between NAND based and NOR based ROM array. Draw the CMOS circuit for 4-bit * 4-bit NOR based ROM array, which stores the following 4 bits in the respective rows.
Row (0) = 0101; Row (1) = 1011; Row (2) = 0110; Row (3) = 0011 (10)
- Q5.a Draw and explain the working of clocked NOR based JK latch circuit using CMOS logic (10)
- b. Compare SRAM with DRAM. Draw 6T SRAM Cell and explain its read and write operations (10)
- Q6. Write short note on any four of the following (20)
- a. NORA logic design style
 - b. Non-volatile Memories-ReRAM
 - c. Carry Save Adder
 - d. Noise margin of Symmetric CMOS inverter
 - e. Interconnect Scaling
