Duration: 3hrs **[Max Marks:80]**

N.B. : (1) Question No 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

1 Attempt any FOUR [20]

a Describe the pinch-off condition in JFET with neat labeled diagram.

b Write a short note on memristors. Include suitable neat sketches wherever necessary.

c With neat sketch describe operation of the capacitor (C) filter with appropriate waveforms.

d Explain the concept of DC load line & Q – Point in bipolar junction transistor (BJT).

e For the circuit shown below in Fig. 1 draw output waveform if an input signal of 20V peak-to-peak is applied.

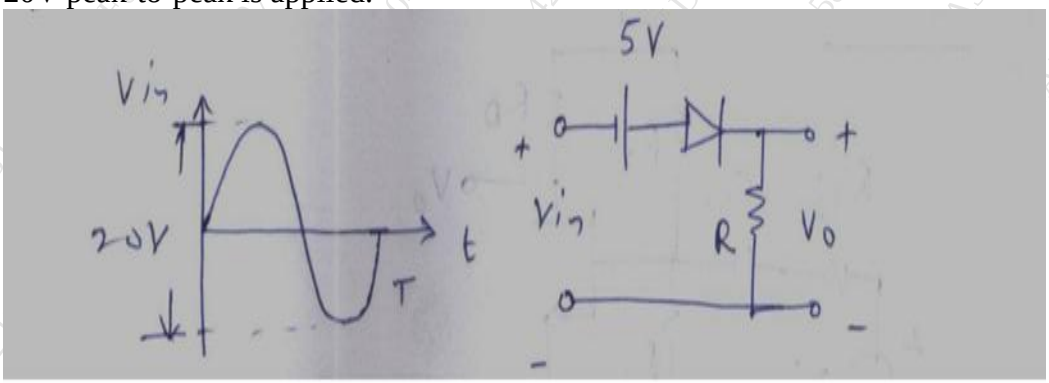

Fig. 1 for Q.1 (e)

2 a Describe the working or operation of a bridge type full wave rectifier with a neat sketch. Draw the output voltage waveforms & mention the expression for DC or average output voltage (Vdc) [10]

b With a neat sketch, explain the Zener diode as a voltage regulator. Describe its operation for both, varying load resistance with a constant DC supply voltage & a varying DC supply voltage with a constant load resistance. [10]

3 a Explain how a PN junction is formed with a neat diagram. [10]

b Explain with the help of neat diagram construction, working & VI characteristics of n channel JFET. [10]

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4	a	Draw a circuit diagram of common source (CS) E-MOSFET amplifier, derive equation of voltage gain (Av), input resistance (Ri) & output resistance (Ro)?	[10]
	b	For small signal amplifier in common emitter (CE) BJT configuration using voltage divider biasing perform small signal (AC) analysis using the hybrid – π model.	[10]
5	a	With a neat sketch, write a short note on solar cell describing its structure or construction, working & V-I characteristics. Mention few real-life applications of solar cells	[10]
	b	Draw circuit diagram and explain the operation of different biasing circuits used for E-MOSFET.	[10]
6	a	Explain construction and working principle of Single Electron Transistor.	[10]
	b	Draw all the different biasing circuits of BJT. Derive the expression of stability factor (SI) for the voltage divider biasing circuit.	[10]

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