(03 Hours) **Total Marks (80)**

Note:

1) Question No 1 is Compulsory.
2) Answer any three from the remaining questions.
3) Assume suitable data wherever required

Q1. Solve **any four** of the following **(20)**

a. Compare Full Custom and Semi-Custom design.

b. Write short note on Static CMOS Design

c. Implement the function F= $\overline{((D+E+A).(B+C))}$using standard CMOS logic

d. Implement 4 X 4 NAND based ROM array.

e. Write short notes on Sense Amplifier.

Q2.a Explain Constant Voltage and Constant Field Scaling in detail with their advantages and disadvantages. **(10)**

b. Explain CMOS inverter characteristics mentioning all regions of operation. **(10)**

Q3.a Compare Pass transistor logic, NMOS logic and CMOS logic. **(10)**

b. Explain read and write operation of 1 T DRAM cell. **(10)**

Q4.a What are the drawbacks of dynamic CMOS logic? Show the modification in dynamic CMOS logic to overcome its drawback. **(10)**

b. Calculate noise margin of a CMOS inverter with the given parameters: **(10)**
NMOS $V_{TO,n}$ =0.6V, u_nC_{ox} = 60 uA/V^2, (W/L)n = 8,
PMOS $V_{TO,p}$ = -0.7V, u_nC_{ox} = 20 uA/V^2, (W/L)p = 12,
V_{DD} =3.3 V.

Q5.a Draw JK flip flop using CMOS and explain the working. **(10)**

b. Draw Carry Look Ahead Adder chain using Dynamic CMOS Logic. **(10)**

Q6. Solve **any 4 out of 5** carry equal marks **(20)**

a. Channel Length Modulation

b. Noise Margin

c. Pseudo -n-MOS

d. 4 X 4 Barrel Shifter

e. Flash Memory

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