Time: 3 Hours **Max. Marks: 80**

N.B.: (1) Question No. **1 is compulsory**.
(2) Solve any **three questions** from the **remaining five**
(3) Figures to the right indicate full marks
(4) Assume suitable data if necessary and mention the same in answer sheet.

Q. 1. Solve any four Questions out of five

A a) Perform the following operation using 2's compliment **[5]**

i) $(35)_{10} - (45)_{10}$

ii) $(45)_{10} - (35)_{10}$

Comment on results of (i) and (ii)

B If $F(A,B,C) = \sum m(1,3,4,5,6) + d(0,2)$ with its truth table and express F in SOP and POS form **[5]**

C Convert D flip flop to T flip flop. **[5]**

D Explain Static RAM **[5]**

E Design Full Adder using VHDL **[5]**

Q. 2. Solve the following

A Prove that NAND and NOR gates are Universal gates **[10]**

B Convert the following into BCD and OCTAL code **[10]**
i) $(7AB)_{16}$ ii) $(125)_{10}$

Q.3. Solve any Two Questions out of Three

A Draw and explain a neat circuit diagram of BCD adder **[10]**

B Design a 3 – bit synchronous counter using J-K FLIP-FLOPs **[10]**

C Realize the following functions of four variables using 8:1 multiplexer **[10]**
F = Σm(0, 1, 2, 3,7, 9, 10, 11, 13, 14, 15)

Q. 4. Solve the following

A What are shift registers? How are they classified? Explain working of SISO type of shift register. **[10]**

B Explain Full Adder circuit using PLA having three inputs, 8 product terms and two outputs. **[10]**

Q. 5. Solve the following

A Draw and explain 4- bit Johnson counter **[10]**

B Draw and explain 3 bit asynchronous binary counter using positive edge triggered JK flip flop. **[10]**

Q. 6. Solve the following

A Compare TTL and CMOS logic families **[05]**

B Convert the following equation in its Canonical form **[05]**
$Y = AB(C + \bar{C}) + A\bar{C}(B + \bar{B}) + BC(A + \bar{A})$

C Simplify the following expression using Boolean algebra **[05]**
Y (A,B, C) = Σm(0,1,2,3,4,5,6,7)

D Compare Moore and Mealy Machine with neat Diagram **[05]**

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